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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,524	08/09/2000	Hiroyuki Takahashi	P19483	5635

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,524	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 21st of April 2004. Claims 1, 2, 6 and 7 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Non-Final Office Action was mailed on 21st of January 2004. Currently, claims 1-7 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for scrapping return-address, temporarily stored in the stack memory area of the RAM, without being restored into the program counter, and jumping to the instruction for calling the next subroutine (See Application, page 70, lines 1-15, and Fig. 31, steps J3 and J4), does not reasonably provide enablement for setting return-address data in the program counter to coincide with the comparison address data (viz., address data of the defective part in the ROM) when execution of the interruption-process is completed (See Claim 1, lines 23-25) for virtually revising the programs stored in the read-only memory (See Claim 1, lines 7-10). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. Moreover, the claim 1 recites the limitation "an address-coincidence-disabler that disables the coincidence between the comparison address data and the return-address set in the program counter by said return-address-setter", which causes that the claimed invention cannot achieve the objective of the applicant's invention, such that the objection of the applicant's invention is to provide a microcomputer with a program-revision ability, wherein a revision can be made in an optional location of programs stored in a ROM thereof (See Application, page 4, line 23 through page 5, line 1), because

said controller/calculator (i.e., CPU) would fetch and execute the defective part of ROM after completion of the revision execution, i.e., the program counter has been set said comparison address data (i.e., address data of the defective part in ROM) as the return address of the interrupt-processing when the interruption-processing has been completed, and furthermore, the address-coincidence-disabling system disables the coincidence between the comparison address data and the return-address set in said program counter by said return-address-setter, i.e., making the controller/calculator fetch and execute the defective part of ROM. The claims 2-7 are dependent claims of the claim 1.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, because the claim 1 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In lines 25-26, the Applicant recites the limitation "when the revisional program adds a program". However, the original specification does not describe the subject matter "revisional program" adds the subject matter "program". The claims 2-7 are dependent claims of the claim 1.

Therefore, the limitation "a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of the interruption-process in accordance with the revisional program is complete and when the revisional program adds a program" in lines 23-26 of the claim 1 could be considered as --a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of the interruption-process in accordance with the revisional program is complete, wherein the revisional program is an additional part of the programs-- for the purpose of the claim rejection based on a prior art since the claims 1-7 are rejected under 35 U.S.C. § 112, first paragraph about scope enablement and new matter issue.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. [US 6,237,120 B1; hereinafter Shimada] in view of what was well known in the art, as exemplified by Crouse et al. [US 4,831,517; hereinafter Crouse].

Referring to claim 1, Shimada discloses a microcomputer (i.e., electronics apparatus in Fig. 2) including a read-only memory (i.e., ROM 15 of Fig. 2) that stores programs (i.e., firmware; See col. 3, lines 55-57 and 61-63), a controller/calculator (i.e., CPU 14 of Fig. 2) that successively accesses to addresses of said programs (i.e., firmware) stored in said read-only memory (i.e., ROM) to retrieve and decode an instruction from said accessed addresses, to execute a process based on said decoded instruction (See col. 1, lines 28-32), and a program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) in which an address to be accessed by said controller/calculator is successively renewed, (See col. 3, lines 39-40 and col. 6, lines 41-45), said microcomputer comprising: at least one comparison-address-storage device (i.e., correcting address storing unit 3 of Fig. 1, which corresponds 16-bit interruption generating address register 21 of Fig. 2) that stores comparison address data (i.e., correcting address) corresponding to an optional address of said programs stored in said read-only memory (i.e., address of defective portion of the firmware stored in ROM; See col. 3, lines 51-59), at which an interruption-process is executed to virtually revise said programs stored in said read-only memory (See col. 4, lines 23-34); a random-access memory (i.e., RAM 26 of Fig. 2) that stores a revisional program (i.e., additional part of the program for correcting contents in ROM) in which said interruption-process is programmed (See col. 4, lines 7-9); at least one vector-address-storage device (i.e., interruption vector register 23b of Fig. 2) that stores a vector address (i.e., interruption vector) data corresponding to a head address (i.e., leading address of said correcting content stored in RAM) of said

revisional program stored in said random-access memory (See col. 4, lines 35-38); and an address comparator (i.e., comparator 22 of Fig. 2) that compares said comparison address data (i.e., correcting address) with an address successively renewed in said program counter (i.e., execution address on Address Bus 16; See col. 4, lines 12-15); wherein said controller/calculator (i.e., CPU) accesses said head address of said revisional program (i.e., leading address of patch for correcting contents in RAM), stored in said random-access memory, corresponding to said vector address data stored in said vector-address-storage device (See col. 4, lines 31-34), when there is a coincidence between said comparison address data and said renewed address of said program counter (See col. 4, lines 12-17), resulting in an execution of said interruption-process in accordance with said revisional program (See col. 4, lines 31-52); a return-address-setter (i.e., ST8 and ST9 in Fig. 3B) that sets return-address data in said program counter when execution of the interruption-process in accordance with the revisional program is complete (See col. 5, lines 16-27); and an address-coincidence-disabler (i.e., switch 24 of Fig. 2) that disables said coincidence between said comparison address data and said return-address set in said program counter by said return-address-setter (i.e., the coincidence signal is disabled by the switch open; See col. 4, lines 27-34).

Shimada does not expressly teach said return-address data coincides with said comparison address data, and said revisional program is an additional part of said programs.

The Examiner takes Official Notice that said return-address-setter that sets return-address data in said program counter to coincide with said comparison address data when execution of said interruption-process in accordance with said revisional program is complete, wherein said revisional program is an additional part of programs, is well known to one of ordinary skill in the art, as evidenced by Crouse (See Figs. 5 and 7, col. 7, line 52 through col. 8, line 36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have coincided said return-address data with said comparison address data for adding said revisional program to said programs since it would allow that said program stored in said read-only

memory (e.g., a single line of ROM code) are expanded into a larger program with said added program (i.e., multiple instructions) by means of said revisional program (i.e., a few instructions) in the patch space in said random-access memory (i.e., read-write memory), which is disclosed by Crouse, at col. 2, line 66 through col. 3, line 2.

Referring to claim 2, Shimada teaches a discriminator (i.e., control flag latch 23a of Fig. 2) that discriminates whether said coincidence between said comparison address data and said renewed address of said program counter is proper (See col. 4, lines 23-27; i.e., the control flag latch (discrimination system) indicates (discriminates) whether a defective portion exists within the ROM (i.e., said coincidence is proper)); and said address-coincidence-disabler (i.e., switch 24 of Fig. 2) further disables said coincidence between said comparison address data and said renewed address of said program counter (i.e., the coincidence signal is disabled by the switch open; See col. 4, lines 27-34).

Referring to claim 3, Shimada teaches a rewritable and non-volatile memory (i.e., EEPROM 27 of Fig. 2) that stores said revisional program, said comparison address data and said vector address data (See col. 4, lines 56-57); a reading/writing system (i.e., communication circuit 29 of Fig. 2) that reads said revisional program, said comparison address data and said vector address data from said rewritable and non-volatile memory, and writes said revisional program, said comparison program, said comparison address data and said vector address data in said random-access memory (See col. 4, lines 7-9), said comparison-address-storage device and said vector-address storage device, respectively (See col. 3, line 66 through col. 4, line 11), whenever said microcomputer is powered ON (See col. 6, lines 1-7).

Referring to claim 4, Shimada teaches said address comparator (i.e., comparator 22 of Fig. 2) is connected to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) to retrieve said renewed address (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Referring to claim 5, Shimada teaches said address comparator (i.e., comparator 22 of Fig. 2) is connected to an address bus (i.e., Address Bus 16 of Fig. 2) extending to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2), to retrieve said renewed address from said program counter (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Referring to claims 6 and 7, Shimada teaches a vector-address data setter (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-storage device, and sets said vector-address-data in said program counter (See col. 3, lines 46-49, and col. 4, lines 30-34; i.e., wherein in fact that the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in the interrupt control unit implies that said vector-address data setter reads said vector address data from said vector-address-storage device, and sets said vector-address-data in said program counter), enabling access to said head address of said revisional program (i.e., leading address of patch for correcting contents in RAM) by said controller/calculator (i.e., CPU; See col. 3, lines 46-49), and execution of said interruption-process in accordance with said revisional program (See col. 4, lines 31-34).

Shimada does not expressly show a vector-address-temporary-storage device that receives said vector address data from said vector-address-storage device, when said address comparator determines that there is coincidence between said comparison address data and said renewed address of said program counter. However, Shimada discloses said vector-address-storage device (i.e., interruption vector register 23b with 16-bits width in Fig. 2) coupled to a data bus (i.e., data bus 13 with 8-bits width in Fig. 2) is loaded into said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) coupled to an address bus (i.e., Address Bus 16 with 16-bits width in Fig. 2). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said

vector-address-temporary-storage device in said controller/calculator (i.e., CPU 14 of Fig. 2), which receives said vector-address data from said vector-address-storage device, when said address comparator determines that there is said coincidence between said comparison address data and said renewed address of said program counter (i.e., when the interrupt occurs) since said data bus (8-bits width) cannot support a direct transfer (viz., single transferring transaction) of said vector address data (16-bits width) from said vector-address-storage device (16-bits width) to said program counter (16-bits width) without said vector-address-temporary-storage device, which could be temporarily holding (viz., buffering) and assembling two 8-bits width said vector-address data into a single 16-bits width said vector-address data for said 16-bits width said program counter and its coupled address bus.

Therefore, Shimada impliedly teaches said vector-address data setter (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-temporary-storage device, and sets said vector-address-data in said program counter (See col. 4, lines 30-34; i.e., wherein in fact that the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in the interrupt control unit implies that said vector-address data setting system reads said vector address data from said vector-address-temporary-storage device, and sets said vector-address-data in said program counter).

Response to Arguments

5. Applicant's arguments filed on 21st of April 2004 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... The presently amended claim 1 recites that the return-address is set in the program counter by the return-address-setter when the revisional program is completed and when the revisional program adds a program. Applicant submits that this clarifies the claim language and addresses the Examiner's concerns as discussed in the above-noted

interview in that the return-address is not set in the program counter by the return-address-setter when there is a bug in the program. ... It thus respectfully asserted that the specification does contain a written description of the invention, ... " on the Response pages 6-8, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, the amended claim 1 does not clarify the claim language and addresses the Examiner's concerns as discussed in the interview conducted on 23rd of March 2004. In the interview, the Examiner was concerning about the claim language "virtually revise" in the claim 1 (See Interview Summary; paper no. 12). However, the Applicant does not reflect the Examiner's concerns to the amended claim 1. Instead, the Applicant introduces a new matter "said revisional program adds a program", which was not disclosed in the original specification. In other words, the Applicant didn't have possession of the claimed invention in the amended claim 1 at the time the application was filed. Moreover, the amended limitation in the claim 1, i.e., a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of the interruption-process in accordance with the revisional program is complete and when the revisional program adds a program, could not overcome the claim rejection under 35 U.S.C. § 112, first paragraph about scope enablement because the specification (See Application, page 70, lines 1-15, and Fig. 31, steps J3 and J4) does not reasonably provide enablement for setting return-address data in the program counter to coincide with the comparison address data (viz., address data of the defective part in the ROM) when execution of the interruption-process is completed (See Claim 1, lines 23-25) for virtually revising the programs stored in the read-only memory (See Claim 1, lines 7-10).

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/ CEL

Sumati Lefkowitz
SUMATI LEFKOWITZ
PRIMARY EXAMINER